UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,845,458 B2
APPLICATION NO. : 10/731679
DATED : January 18, 2005
INVENTOR(S) : Feng Lin

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the TITLE page, Item (54) please change the title from "SYSTEM AND METHOD OF OPERATION OF DLL AND PLL TO PROVIDE TIGHT LOCKING WITH LARGE RANGE, AND DYNAMIC TRACKING OF PVT VARIATIONS USING INTERLEAVED DELAY LINES"

and insert therefore -- SYSTEM AND METHOD OF OPERATION OF DLL (DUAL LOCKED LOOP) AND PLL (PHASE LOCKED LOOP) TO PROVIDE TIGHT LOCKING WITH LARGE RANGE, AND DYNAMIC TRACKING OF PVT VARIATIONS USING INTERLEAVED DELAY LINES --.

The title page, showing the illustrative figure, should be deleted and substitute therefore the attached title page.

The drawing sheets, consisting of Figs 1-10, should be deleted to be replaced with drawing sheets consisting Figs. 1-10, as shown on the attached pages.

In the text, correct the following:

Column 1:

lines 1-5, delete "SYSTEM AND METHOD OF OPERATION OF DLL AND PLL TO PROVIDE TIGHT LOCKING WITH LARGE RANGE, AND DYNAMIC TRACKING OF PVT VARIATIONS USING INTERLEAVED DELAY LINES" and insert -- SYSTEM AND METHOD OF OPERATION OF DLL (DUAL LOCKED LOOP) AND PLL (PHASE LOCKED LOOP) TO PROVIDE TIGHT LOCKING WITH LARGE RANGE, AND DYNAMIC TRACKING OF PVT VARIATIONS USING INTERLEAVED DELAY LINES --.

line 66, before "phase" insert -- or --.

Column 2:

line 2, delete "rang" and insert therefore -- range --.

line 47, after "device" insert -- ; --.

Column 3, line 5, delete "if" and insert therefore -- in --.

Column 4, line 17, delete "is".

In the claims, correct the following:

Column 7:

claim 1, line 14, delete "o" and insert therefore -- of --.

claim 2, line 3, delete "intrinic" and insert therefore -- intrinsic --.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,845,458 B2
APPLICATION NO. : 10/731679
DATED : January 18, 2005
INVENTOR(S) : Feng Lin

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 8:

claim 17, line 2, delete "as" and insert therefore -- has --.
claim 19, line 8, after "circuit" insert -- path --.
claim 19, line 8, delete "the" first occurrence.
claim 19, line 13, delete "in".
claim 21, line 10, delete "track" and insert -- tracks --.
claim 21, line 18, delete "o" and insert -- of --.

Column 9, claim 28, line 3, delete "de ay" and insert therefore -- delay --.

Column 10, claim 39, line 12, after "circuit" insert -- path --.

Column 11:

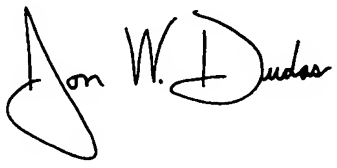
claim 42, line 5, delete "trinsic" and insert therefore -- intrinsic --.
claim 43, line 8, delete "an" and insert therefore -- and --.
claim 44, line 7, delete "associate" and insert therefore -- associated --.
claim 46, line 11, delete "an" and insert therefore -- and --.

Column 12:

claim 47, line 9, delete "an" and insert therefore -- and --.
claim 49, line 12, delete "an" and insert therefore -- and --.

Signed and Sealed this

First Day of July, 2008



JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Lin

(10) **Patent No.: US 6,845,458 B2**
(45) **Date of Patent: Jan. 18, 2005**

(54) **SYSTEM AND METHOD OF OPERATION OF DLL AND PLL TO PROVIDE TIGHT LOCKING WITH LARGE RANGE, AND DYNAMIC TRACKING OF PVT VARIATIONS USING INTERLEAVED DELAY LINES**

(75) Inventor: **Feng Lin**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/731,679**

(22) Filed: **Dec. 9, 2003**

(65) **Prior Publication Data**

US 2004/0119512 A1 Jun. 24, 2004

Related U.S. Application Data

(62) Division of application No. 09/652,632, filed on Aug. 31, 2000.

(51) **Int. Cl.**[7] **G06F 1/12**

(52) **U.S. Cl.** **713/401**; 713/400; 713/401; 713/500; 713/503; 327/147; 327/149; 327/157; 327/158; 327/161

(58) **Field of Search** 713/400, 401, 713/500, 503; 327/147, 149–163; 716/6; 375/375–376

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,165,490	A		8/1979	Howe et al.
5,003,562	A	*	3/1991	van Driest et al. 375/327
5,109,394	A		4/1992	Hjerpe et al.
5,192,886	A		3/1993	Wetlaufer
5,198,758	A		3/1993	Iknaian et al.
5,272,390	A		12/1993	Watson et al.
5,369,640	A		11/1994	Watson et al.
5,420,531	A	*	5/1995	Wetlaufer 327/270
5,544,203	A		8/1996	Casasanta et al.
5,552,726	A		9/1996	Wichman et al.
5,604,775	A		2/1997	Saitoh et al.
5,638,010	A		6/1997	Adams
5,774,403	A		6/1998	Clark et al.
5,787,132	A	*	7/1998	Kishigami et al. 375/354
5,790,612	A		8/1998	Chengson et al.
5,808,478	A	*	9/1998	Andresen 326/31
5,844,954	A		12/1998	Casasanta et al.
5,870,003	A		2/1999	Boerstler
5,923,715	A	*	7/1999	Ono 375/376
5,925,133	A	*	7/1999	Buxton et al. 713/323
6,011,732	A	*	1/2000	Harrison et al. 365/194
6,047,346	A		4/2000	Lau et al.
6,094,082	A		7/2000	Gaudet
6,101,197	A		8/2000	Keeth et al.
6,121,808	A		9/2000	Gaudet
6,131,168	A		10/2000	Krzyzkowski
6,204,732	B1		3/2001	Rapoport et al.
6,259,295	B1	*	7/2001	Kriz et al. 327/296
6,268,753	B1		7/2001	Sandusky
6,285,172	B1		9/2001	Torbey
6,445,231	B1	*	9/2002	Baker et al. 327/158
6,462,623	B1		10/2002	Horan et al.
6,480,047	B2		11/2002	Abdel-Maguid et al.
6,518,812	B1	*	2/2003	Sikkink et al. 327/284
6,718,477	B1	*	4/2004	Plants et al. 713/500

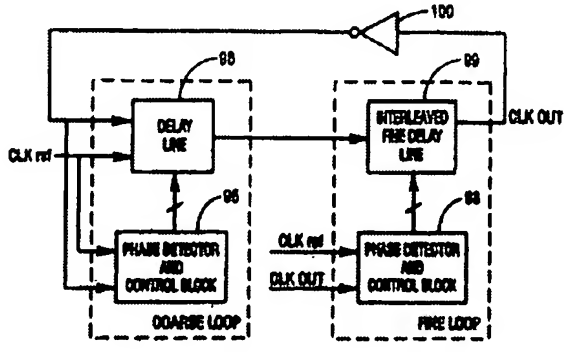
* cited by examiner

Primary Examiner—Lynne H. Browne
Assistant Examiner—Nitin C. Patel
(74) *Attorney, Agent, or Firm*—Thorp Reed & Armstrong LLP

(57) **ABSTRACT**

An interleaved delay line for use in phase locked and delay locked loops is comprised of a first portion providing a variable amount of delay substantially independently of process, temperature and voltage (PVT) variations while a second portion, in series with the first portion, provides a variable amount of delay that substantially tracks changes in process, temperature, and voltage variations. By combining, or interleaving, the two types of delay, single and dual locked loops constructed using the present invention achieve a desired jitter performance under PVT variations, dynamically track the delay variations of one coarse tap without a large number of delay taps, and provide for quick and tight locking. Methods of operating delay lines and locked loops are also disclosed.

50 Claims, 5 Drawing Sheets



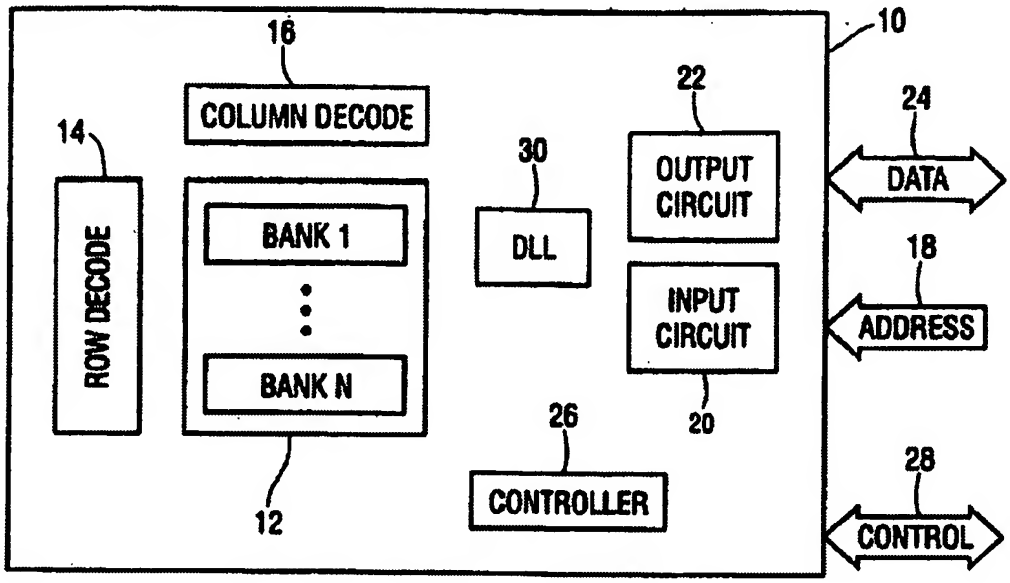

16
COLUMN DECODE
14
ROW DECODE
BANK 1
BANK N
12
30
DLL
22
OUTPUT CIRCUIT
INPUT CIRCUIT
20
26
CONTROLLER
10
24
DATA
18
ADDRESS
28
CONTROL

Fig.1

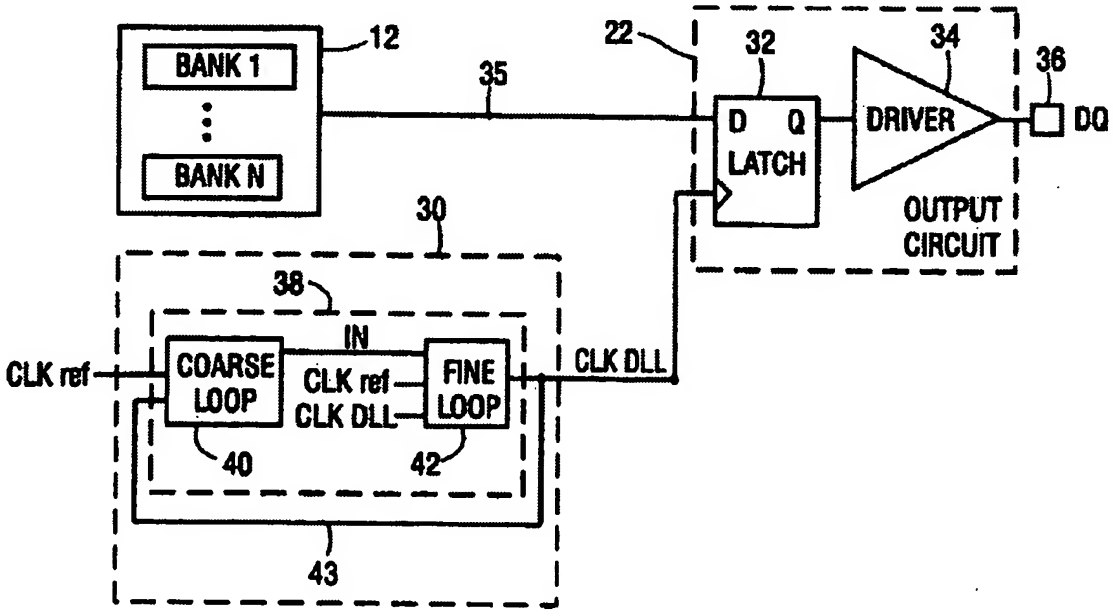

BANK 1
BANK N
12
35
22
32
34
36
D Q
LATCH
DRIVER
DQ
OUTPUT CIRCUIT
30
38
IN
CLK ref
COARSE LOOP
CLK ref
CLK DLL
FINE LOOP
CLK DLL
40
42
43

Fig.2

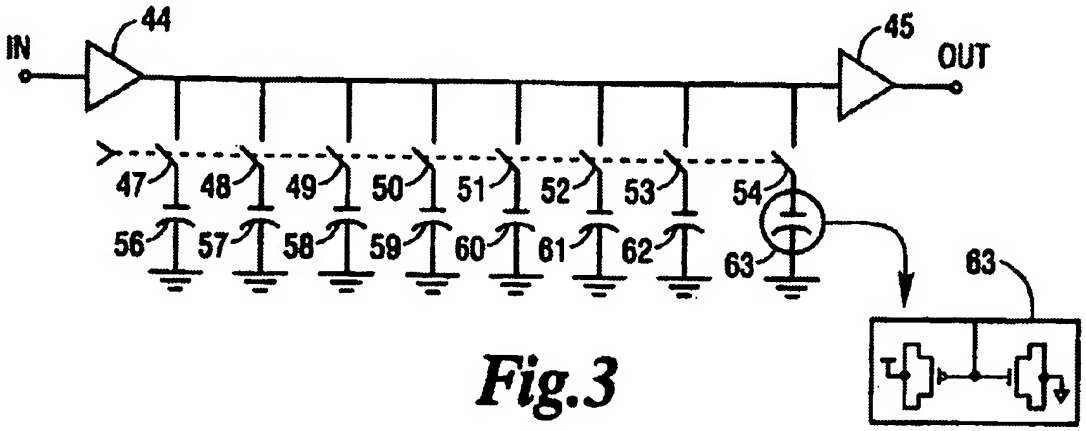


Fig.3

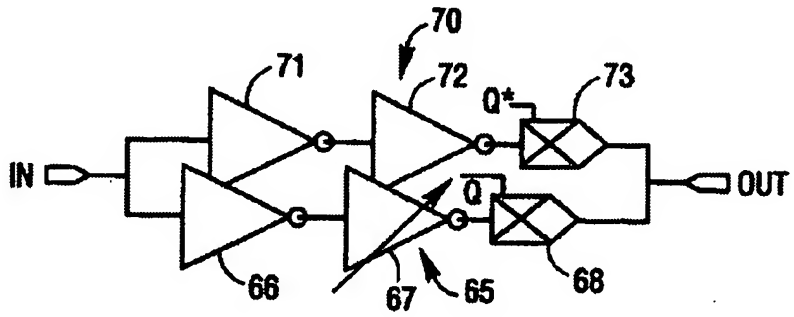


Fig.4

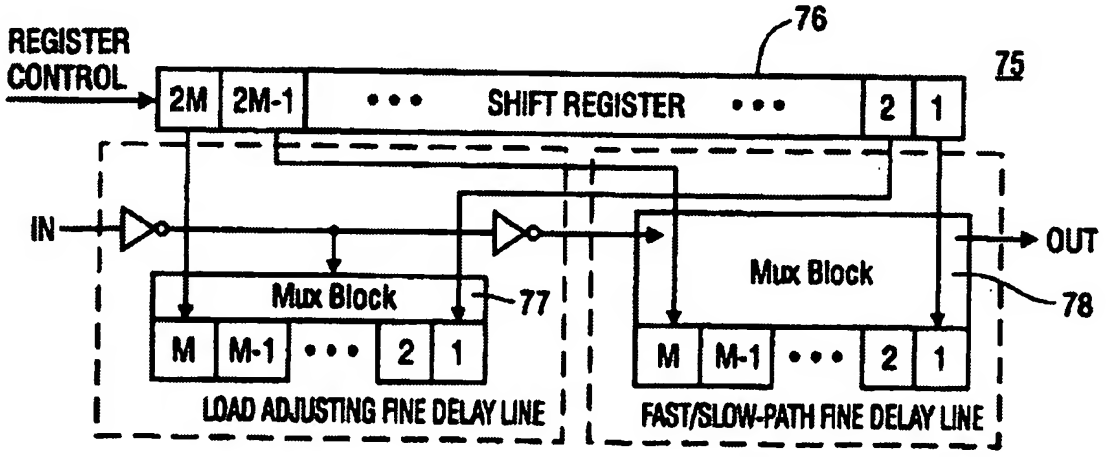


Fig.5

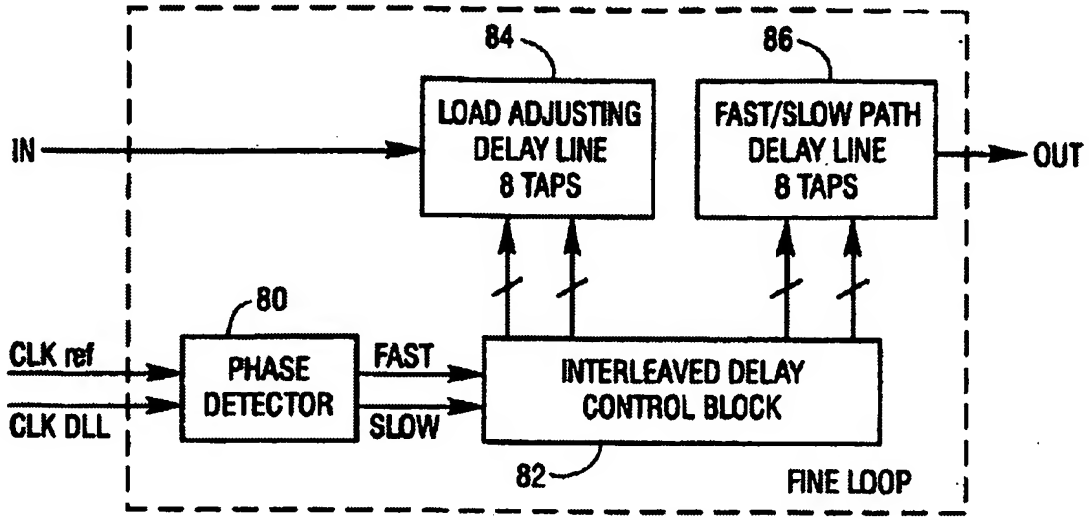


Fig.6

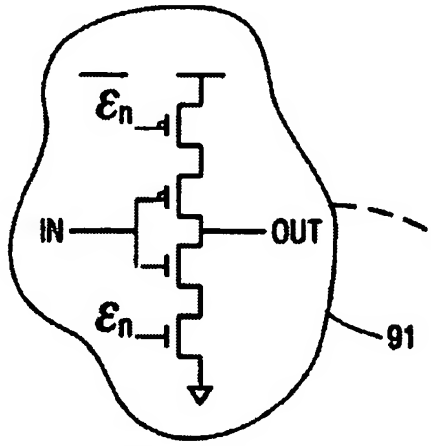


Fig.7A

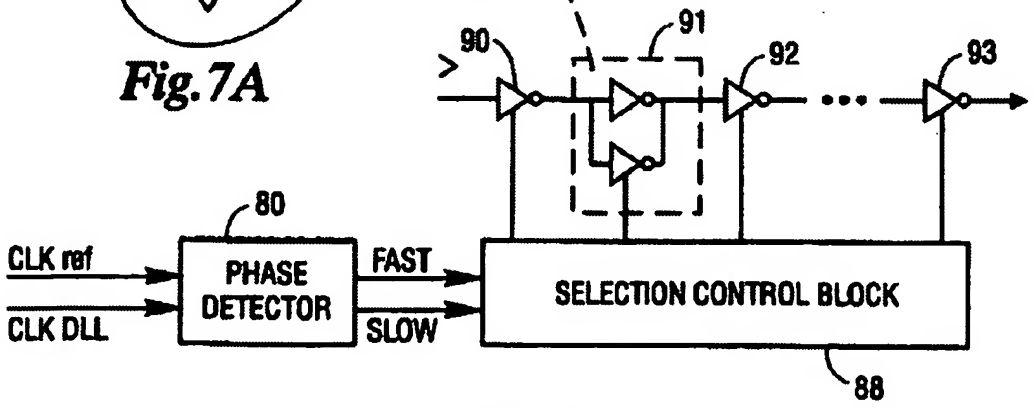


Fig.7

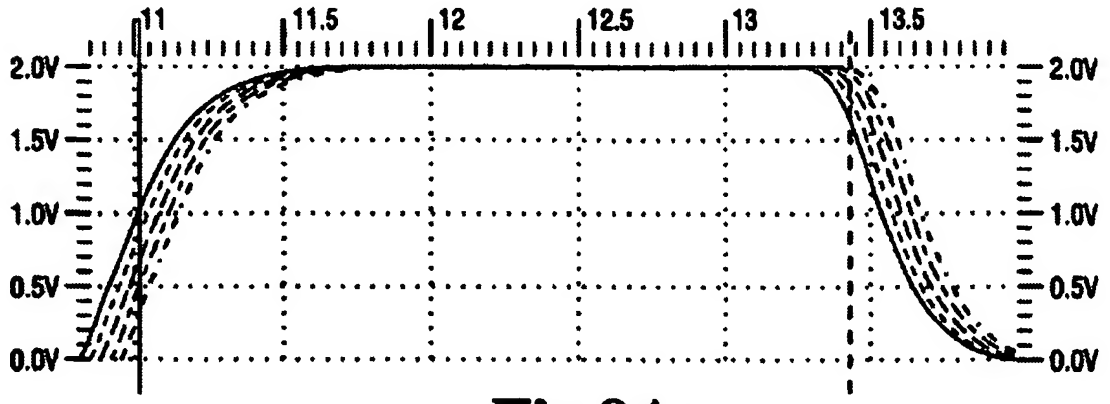


Fig.8A

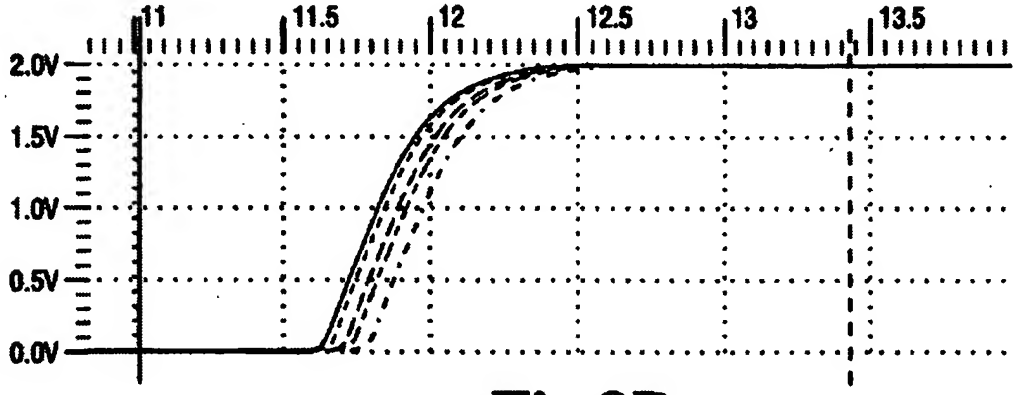


Fig.8B

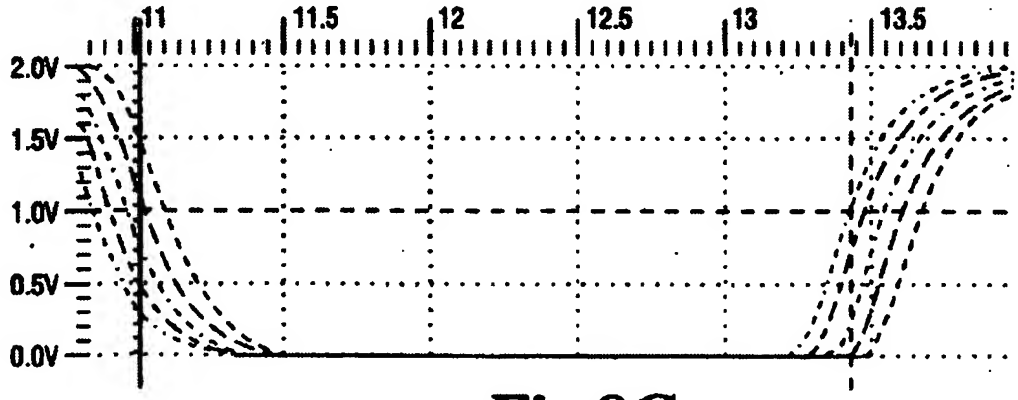


Fig.8C

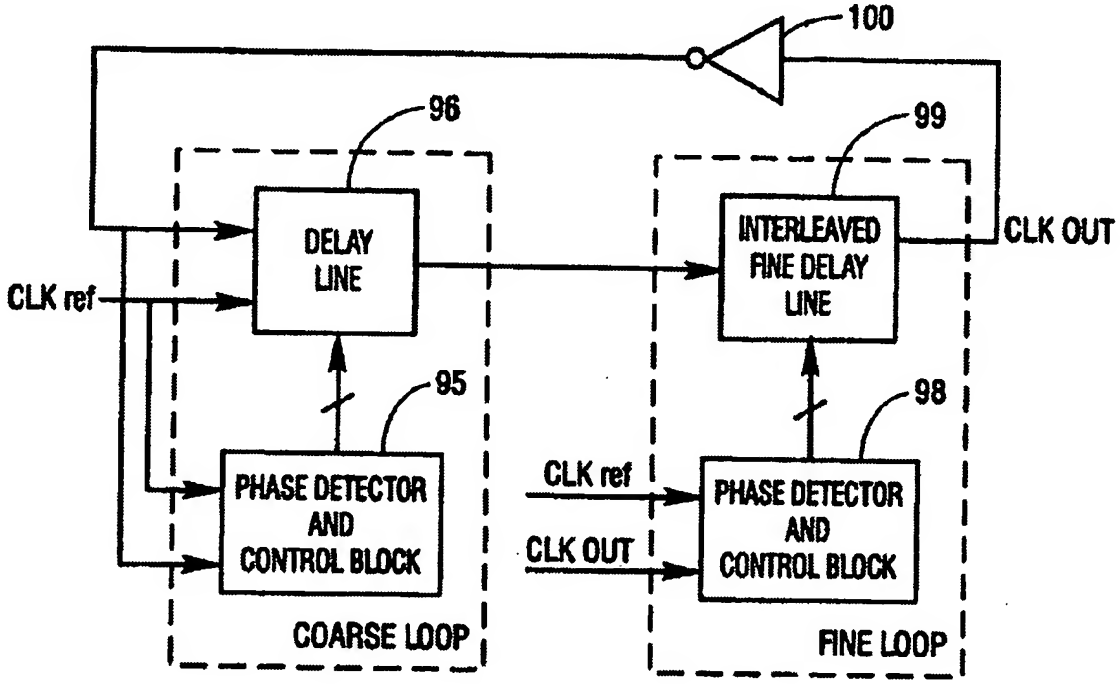

100
96
99
DELAY LINE
INTERLEAVED FINE DELAY LINE
CLK OUT
CLK ref
95
98
PHASE DETECTOR AND CONTROL BLOCK
CLK ref
CLK OUT
PHASE DETECTOR AND CONTROL BLOCK
COARSE LOOP
FINE LOOP

Fig.9

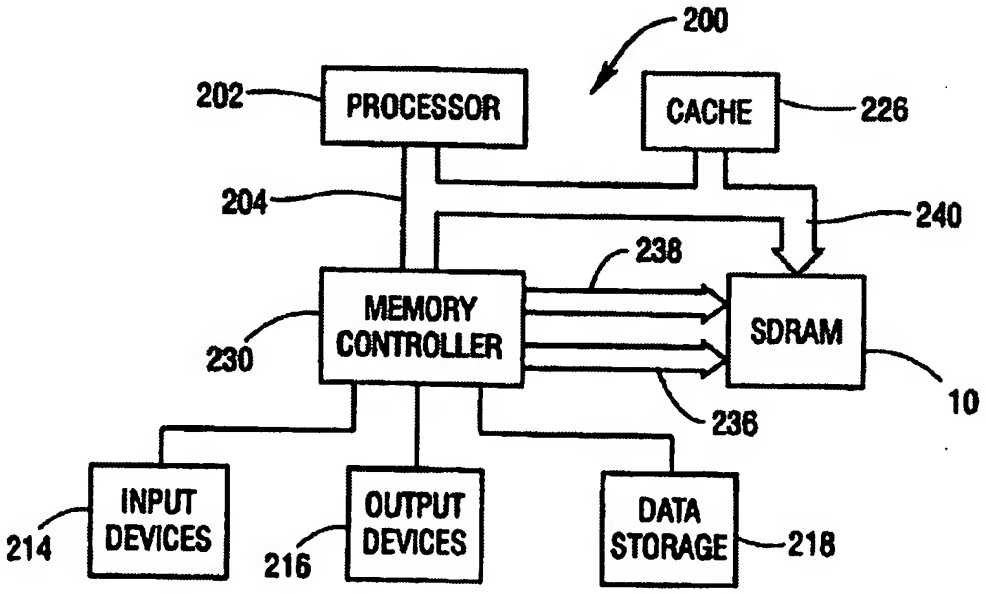

200
202
PROCESSOR
CACHE
226
204
240
238
MEMORY CONTROLLER
SDRAM
230
10
236
INPUT DEVICES
OUTPUT DEVICES
DATA STORAGE
214
216
218

Fig.10